REMARKS

In response to the Official Action mailed June 11, 2003, Applicants propose to amend their application and request reconsideration in view of the foregoing amendment and the following remarks. No claims are added or cancelled so that claims 1, 3, 6, and 8-12 remain pending.

Applicants supplied a corrected PTO-1449 form with the previous amendment for the Information Disclosure Statement that the Examiner acknowledged in the Official Action mailed June 11, 2003. That PTO-1449 form corrected an error in the previous PTO-1449 form, the one returned by the examiner. The foreign publication cited in that Information Disclosure Statement is, as pointed out in the previous amendment, a Korean publication, not a Japanese publication. Correction of the record of this patent application is respectfully requested.

Claims 1, 6, 9, 10, and 12 were rejected as indefinite for lack of antecedent basis for the term "said channel regions", appearing in the final paragraphs of the independent claims 1 and 10. This error is regretted and is corrected in this Amendment. As well known to those of skill in the art, transistors including sources, gates, and drains as described in the patent application and the claims are field-effect transistors that include channel regions. Thus, the description of the channel regions in the amended independent claims is correct and provides appropriate basis for the dependent claims.

Claim 9 was rejected as indefinite because of the reference to "said display area". Antecedent basis is provided in the foregoing amendment of claim 1, overcoming the rejection as to form. Support for this amendment of claim 1 is found in the description of prior art Figure 28 at page 1 of the patent application and at page 6, lines 7-13, for example, of the patent application. Figure 28 shows the display area 102 and the driving circuit areas 111 and 112 along respective sides the display area 102, as described in amended claim 1.

Claim 8 was rejected as indefinite because, according to the Official Action, "there is no labeling as to which [driving transistors] are the first and which ones are the second driving transistors", making it difficult to determine the distance between the first and second driving transistors recited in that claim. This rejection is respectfully traversed.

Claim 8 is clear and need not be amended to overcome the rejection. Claim 8 refers to the distance between first and second driving transistors and specifies which transistor is the second of the transistors, relative to the first of the transistors. The second transistor is the transistor of the driving transistors that neighbors and is positioned nearest to the first driving transistor. This language is quite clear, even read by itself, and particularly when considered in combination with the disclosure of the patent application, including the

drawings. Claim 8 uses language commonly used and accepted in claims in U.S. practice. It merely specifies that if one of the driving transistors is arbitrarily chosen as the first transistor, then the second transistor is determined. That second transistor is determined because it is the driving transistor nearest the first transistor. Having made those designations, the rest of the claim has an unambiguous meaning. Claim 8 meets all of the requirements of 35 USC 112.

Without limiting the scope of claims 8 or 9, Applicants attach pictorial explanations of the application of the questioned language of claims 8 and 9 to the embodiments of Figures 24 and 26 of the patent application, respectively. These drawings and their annotations, based entirely on the disclosure of the patent application show that claims 8 and 9 are readily understood based on the disclosure. The rejection should be withdrawn.

Claims 1, 3, 6, and 10-12 were rejected as unpatentable over Shiraki et al. (U.S. Patent 5,844,538, hereinafter Shiraki et al.). This rejection is respectfully traversed.

Applicants agree with the Examiner's characterization of what is disclosed in Shiraki through the sentence that ends in the fourth line on page 4 of the Official Action. From that point, Applicants contend that the Official Action does not faithfully describe what appears in Shiraki.

As understood, reliance is placed upon Figure 26 of Shiraki, describing a conventional interconnection arrangement in one pixel of a liquid crystal display. That connection arrangement is further explained in Shiraki in combination with at least Figures 24 and 25 of Shiraki. According to the Official Action, Shiraki discloses gate interconnections 105. Applicants agree.

There is a fundamental flaw in the remainder of the comparison made between Shiraki and the invention. The transistors in Shiraki's Figure 26 are not driving transistors as are the transistors of the present claims. Rather, Shiraki's transistors are "picture" transistors that turn on and off in response to the signals supplied by the driving transistors that are the focus of the present invention. Shiraki aims to eliminate an auxiliary capacitor by supplying data to these picture transistors multiple times during a single frame and, also, to increase aperture ratio. Thus, Shiraki is different in structure, i.e., picture transistors versus driving transistors, as well as in function and effect, from the invention.

Even considering the line of reasoning of the Official Action, by reference to Figure 25, it can be seen that the gates of the respective transistors corresponding pixels are connected by respective scan signal lines 105, the same designation used in Figure 26. According to the Official Action, these interconnections are located along respective zigzag patterns. Applicants respectfully disagree.

Figure 26 of Shiraki shows that the interconnections 104, *not 105*, appear along complex paths that might be considered, in some way, to be zigzag paths. Referring again to Figure 25 of Shiraki, it is apparent that the lines 104 are the data signal lines that connect respective sources of the field-effect transistors and respective pixels of the liquid crystal display. Accordingly, contrary to the analysis of the Official Action, considering not only Figure 26 of Shiraki, but also considering Figure 25 of Shiraki, which further explains Figure 26, Shiraki does not describe a gate interconnection of any transistors having the geometric structure described in the rejected claims.

The Examiner conceded that Shiraki does not "explicitly disclose the gate interconnection in Fig. 26", and referred to Figure 9 of Shiraki. However, Figure 9 of Shiraki relates to what Shiraki discloses as his invention (i.e., increased aperture ratio and removal of a capacitor), not to the structure of the conventional liquid crystal display circuitry illustrated in Figures 24-26 of Shiraki. Moreover, reference to Figure 9 of Shiraki shows that the gates of the two transistors depicted there are not connected together. Figure 9 does not illustrate any particular geometrical interconnection. The gates of the two transistors shown in that Figure 9 are connected to respective, i.e., different, scan signal lines 1 and 2. Thus, Shiraki does not disclose anything concerning a gate interconnection in Figure 26 of Shiraki nor even suggest a gate interconnection that is in any way similar to the gate interconnection that is claimed in the present application. For these reasons, the rejection of claims 1, 3, 6, and 10-12 is erroneous.

The Examiner made reference to Sung (U.S. Patent 5,978,058) in the Official Action but does not appear to have made a rejection based upon a proposed modification of Shiraki by Sung. Thus, while Sung may be useful as showing one form of gate interconnection, Sung is not considered to be part of any rejection and does not need any comment. Even if Sung is considered part of a rejection, Sung does not disclose nor suggest modifying the source interconnection in Figure 26 of Shiraki in any way that would be similar to the invention claimed.

Applicants respectfully disagree with the comments appearing at page 5 of the Official Action regarding the dependent claims 3, 6, 11, and 12.

Claims 3 and 11, which include identical limitations, are directed to more complex embodiments of the invention, for example the embodiments shown in Figures 23-27 of the patent application. Since Shiraki does not show a gate interconnection with the relatively simple geometry of claims 1 and 10, it cannot disclose nor suggest the substantially more complex geometry described in the dependent claims 3 and 11.

Claims 6 and 12 have identical limitations specifying that the channel regions of the driving transistors that are interconnected have widths that are parallel to the first and second

straight lines. It would appear that the thin film transistors 107 in Figure 26 of Shiraki have channel widths that are horizontal in that figure. This conclusion is based upon considering Figures 25 and 26 of Shiraki together. Based upon the Examiner's conclusion with respect to the first and second straight lines regarding interconnection 104, it is apparent that these widths are not parallel to either of those lines. However, more importantly, since there is no arrangement of the gate interconnections along zigzag lines in Figure 26 of Shiraki, a comparison that would need to be made in order to determine whether a suggestion for claims 6 and 11 might be present in Shiraki, cannot be made.

For the foregoing reasons, upon reconsideration, the rejections of claims 1, 3, 6, and 10-12 should be withdrawn.

Claims 8 and 9 were rejected as unpatentable over Shiraki in view of Yamazaki et al. (U.S. Patent 5,821,138, hereinafter Yamazaki). This rejection is respectfully traversed.

As an initial matter, the rejection of claims 8 and 9 depends upon the propriety of the rejection of claim 1, from which both claims depend. Since, as already demonstrated, the rejection of claim 1 cannot be properly maintained, the rejection of claims 8 and 9 should be withdrawn.

Yamazaki was relied upon as describing a process of crystallization of amorphous silicon to produce polycrystalline silicon. Applicants do not assert that they have invented such a process and there is no claim to such a process. Rather, Applicants have disclosed a particular use of that process to provide a particularly advantageous result in constructing the driving transistors of a liquid crystal display from polycrystalline silicon. As explained in the patent application, particularly from page 16, line 5 through page 17, line 14, and from page 19, line 21 through page 23, by employing the geometric arrangement of the claimed invention, errors that occur in the crystallization process do not adversely affect the final product. As explained there, typically, re-crystallization with laser light is achieved using a pulsed laser. Occasionally, errors occur in the light pulses and a light pulse is not emitted in response to a trigger signal. By employing zigzag traces of the spot of laser light to produce the claimed invention, defects in the re-crystallization process do not adversely affect the driving transistors that are produced, increasing the yield of the liquid crystal display. Yamazaki does not describe this problem and therefore cannot even contemplate the solution. In other words, even if Yamazaki is employed to modify the disclosure of Shiraki, the structures claimed in claims 8 and 9 would still not be produced. Therefore, *prima facie* obviousness of those claims is not established by the supplemental citation of Yamazaki.

The Examiner made comments with respect to claims 8 and 9 as product-by-process claims, including the ritual citation of *In re Thorpe*. Applicants respectfully point out that claims 8 and 9 make reference to processes that describe strips of a liquid crystal display

apparatus that are produced in the process. The strips are a characteristic of the resulting product and can be discovered by studying the product. In other words, the product does disclose the process employed in manufacturing the claimed product. In this situation, product-by-process claims are independently patentable pursuant to U.S. law. See MPEP 2173.05 (p).

For all of the foregoing reasons, the claims present here should now be allowed.

In the proposed amendment, the only amendments made respond to issues of form. Those amendments improve the form of the claims and thus reduce the issues to be considered in the event of an Appeal. Therefore, even if the Examiner decides to maintain the rejection, the amendment should be entered.

Reconsideration and favorable action are earnestly solicited.

Respectfully submitted,

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